IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re divisional patent application of 10/224,899 filed on August 21, 2002

Clevenger et al.

Serial No.: Not Yet Assigned — Group Art Unit: Unknown

Filing Date: Concurrently Herwith — Examiner: Unknown

For: INTEGRATED METAL-INSULATOR-METAL CAPACITOR METAL GATE TRANSISTOR

Commissioner of Patents
PO BOX 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Under the provisions of 37 CFR §1.97 through §1.99 and pursuant to applicant's duty of disclosure under 37 CFR §1.56, applicant respectfully brings the following documents listed on the attached form PTO-1449, to the attention of the Examiner in charge of the above-identified application. All of these references were either cited or submitted in parent Application No. 10/224,899 and thus copies of these references are not provided in accordance with 37 C.F.R. §1.98(d).

This citation does not constitute an admission that the references are relevant or material to the claims. They are only cited as constituting related art of which the applicant is aware.

It is respectfully requested that the listed references be considered by the Examiner and formally made of record in this application.

YOR920010565US2

Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 50-0510.

Respectfully submitted,

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Date: 2/26/04

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INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

ATTY DOCKET NO.	SERIAL NO.
YOR920010565US2	Not Yet Assigned
Clevenger et al.	
FILING	GROUP
Concurrently Herewith	Unknown

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
		5,903,493	05/11/1999	Lee			
		6,033,963	03/07/2000	Huang et al.			
		6,049,114	04/11/2000	Maiti et al.			
		6,057,583	05/02/2000	Gardner et al.			
		6,130,123	10/10/2000	Liang et al.			
		6,165,858	12/26/2000	Gardner et al.			
		6,198,617	03/06/2001	Sun			
		6,341,056	01/22/02	Allman et al.			
		6,451,667	09/17/02	Ning			
		6,528,834	03/04/03	Durcan et al.			

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

			"New Paradigm of Silicon Technology," Tadahiro Ohmi, et al., Proceedings of the IEEE, Vol. 89, No. 3, March 2001, pp. 394-412
			"Dual-Metal Gate CMOS Technology with Ultrathin Silicon Nitride Gate Dielectric," Yee-Chia Yeo et al., IEEE Electron Device Letters, Vol. 22, No. 5, May 2001, pp. 227-229

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

			"Dual-Metal Gate Technology for Deep-Submicron CMOS Transistor, " Qiang Lu et al., IEEE 2000 Symposium on VLSI Technology Digest of Technical Papers, pp. 72-73

EXAMINER	DATE CONSIDERED

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